REMARKS/ARGUMENTS

Claims 31-34 and 39-43 remain in the application. Claims 1-30 have been canceled and were allowed in the parent application. Claims 35-38 have been cancelled. Claims 31 and 39 has been amended.

Rejections Under 35 U.S.C. §101

Claims 35-38 were rejected under 35 U.S.C. §101 as claiming the same invention as claims 5-8 of U.S. Patent No. 6,651,158. In response, these claims have been cancelled, making this rejection moot.

Rejections Under 35 U.S.C. §112, Second Paragraph

Claims 31-34 and 39-43 were rejected under 35 U.S.C. §112, second paragraph as failing to distinctly claim the invention. With respect to claim 31, the Office Action states that is it unclear how a future event can be determined in the determining operation of that claim. Applicants respectfully disagree that this claim is unclear from its language. The claim language states that based on a current event ("due to processing of instructions for the second thread"), it can be determined whether a future event will take place ("whether instruction fetch operations for the first thread will be blocked"). Given the claim language alone, there should be no confusion as to how the determining operation can be carried out. Moreover, the specification describes examples of this operation (*see, e.g.*, page 8). With respect to the result of that determination, claim 34 has been amended to refer to the assigning of thread priority based on the determining operation. The same objections were made to claim 39, and the arguments above apply to this claim as well. As to the interrelation of the control logic and the thread queues, claim 39 has been amended to refer to the thread queue as storing instructions of a

thread. In view of the above, reconsideration and withdrawal of the rejection of claims 31-34 and 39-43 under 35 U.S.C. §112, second paragraph is respectfully requested.

Claim Rejections Under 35 U.S.C. §102(b)

Claims 31-34 and 39-43 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,018,756 to Doing et al. ("Doing").

According to an embodiment of the present invention, a multi-threaded processor is provided where it is determined (*e.g.*, with control logic) whether instruction fetch operations for a first of two threads will be blocked due to processing of instructions for the second thread. As seen in claim 31, such a determination may be used to assign priority to the first thread in the processor.

Such a feature is not shown in the Doing reference. In Doing, specifically at Col. 19, lines 37-49, it states as follows:

> The three priorities of each thread are high, medium, and low. When the priority of thread T0 is the same as thread T1, there is no effect on the thread switching logic. Both threads have equal priority so neither is given an execution time advantage. When the priority of thread T0 is greater than the priority of thread T1, thread switching from T0 to T1 is disabled for all L1 cache misses, *i.e.*, data load, data store, and instruction fetch, because L1 cache misses are resolved much faster than other conditions such as L2 misses and translates. Thread T0 is given a better chance of receiving more execution cycles than thread T1 which allows thread T0 to continue execution so long as it does not waste an excessive number of execution cycles.

Accordingly, Doing is not looking at instruction fetch operations of a first thread to assign priority to a second thread as called for in claims 31 and 40. As seen from this section of Doing, when thread T0 has a priority greater than thread T1, cache misses for thread T0 will not result in a thread switch to thread T1 nor will it result in a change in assignment of priority as

called for in claims 31 and 40. As to claims 31 and 39, Doing is silent as to determining whether execution of one thread will result in the blocking of processing of instructions of another thread.

In view of the above, reconsideration and withdrawal of the rejection of claims 31-34 and 39-43 under 35 U.S.C. §102(b) is respectfully requested.

Applicants respectfully submit that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (202) 220-4255 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to Deposit Account **No. 11-0600**.

Respectfully submitted,

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By: _____

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